REMARKS

Claims 28–55 are pending and are presented for reconsideration. Claim 45 has been amended to correct a typographical error. Support for the amendment may be found in, e.g., the originally filed claims. No new matter has been added.

Rejection of claims under 35 U.S.C. § 103(a)

Claims 28–55 are rejected under 35 U.S.C. § 103(a) as being unpatentable over K. Ismail, "Si/SiGe High-Speed Field Effect Transistors," *IEEE IEDM Tech. Dig.*, pp. 509-512, 1995 ("Ismail") in view of Chang et al., "Selective Etching of SiGe on SiGe/Si Heterostructures," *J. Electrochem Soc.*, Vol. 138, No. 1, pp. 202-204, January 1991 ("Chang"). Ismail appears to disclose designs for SiGe-based modulation-doped field-effect transistors and metal-oxide-semiconductor field-effect transistors. *See* Ismail, Figured 7, 9, and related text. Chang appears to disclose methods for selectively etching SiGe over Si. *See* Chang, abstract. The Examiner relies on Ismail to teach all of the limitations of independent claims 28 and 46. The Examiner recognizes that Ismail does not disclose selectively removing a SiGe layer to expose a strained semiconductor layer, and relies on Chang to supply this feature.

Ismail is utterly silent about any method utilized to form his structures of Figure 7 and 9, because he has not physically fabricated them. Figures 7 and 9 are simply schematics of structures existing only in circuit-performance models. *See* Ismail, p. 510, right column, bottom paragraph and page 511, left column, bottom paragraph. The Examiner erroneously infers Applicants' methods by applying the etch step disclosed by Chang to the model illustrated in Figure 7 of Ismail, when in fact, Ismail's structure may be fabricated in other ways. For example, rather than selectively removing layers from his N-MODFET structure (right side of Figure 7), Ismail could selectively add layers to his P-MODFET structure (left side of Figure 7). The Federal Circuit has repeatedly held that the relevance of a reference cannot be predicated on "mere conjecture." In re Robinson W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851, 105 S.Ct. 172 (1984); Continental Can Co. v. Monsanto Co., 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991) ("The mere fact that a certain thing may result from a given set of circumstances is not

sufficient"). Here, the Examiner has cited Ismail, in combination with the method disclosed by Chang, for a proposition it plainly does not disclose.

Moreover, one of skill in the art would not utilize Chang's method to attempt to form Ismail's structure. Firstly, Chang's approach would not achieve the straight vertical feature profile Ismail shows in Figure 7. Chang discloses only wet etches that are known to those of skill in the art as being isotropic etches. Thus, removing the layers as suggested by the Examiner would result in a ragged, undercut sidewall profile. In order to make Ismail's structure by selective removal as suggested by the Examiner, one would require an anisotropic etch to achieve the illustrated straight sidewall. Moreover, evenly exposing both i-Si and the n+ regions on the right side of Ismail's structure requires an etch that is equally selective to both doped and undoped material. As Chang himself discloses, a difference in doping concentrations may result in a variation in etch rates of 10–20%. *See* Chang, p. 203, left column, first partial paragraph. This etch rate variation would preclude the formation of the smooth top surface of the right side of the device shown in Ismail, Figure 7. Finally, selective removal of material to form Ismail's structure may require the removal of n+ doped regions from the right side of Ismail's structure. Chang only discloses a solution for the selective removal of highly doped p–type SiGe. *See* Chang, page 204, Summary. Thus, the method disclosed by Chang cannot be used to form structures with the features illustrated by Ismail.

Furthermore, regarding claim 46, Ismail does not teach or suggest forming a gate dielectric over a strained semiconductor layer and selective removal of SiGe disposed over the strained semiconductor layer. Rather, Ismail discloses only Schottky diodes, in contrast to insulated gates, in combination with the structure of Ismail's Figure 7 – i.e., the structure that the Examiner asserts is obvious to form by selective etching. Ismail does disclose a gate dielectric in the model illustrated in Figure 9, but the planar structure of Figure 9 includes a pure Si cap layer on which the gate oxide can be formed. *See* Ismail, p. 511, left column, bottom paragraph. Adding a Si cap layer to the structure of Ismail's Figure 7 would alter the configuration of the device and may render that device inoperable, as the device is shown as having exposed SiGe sidewalls that may be required for device functionality. Moreover, Ismail relies on the planarity of the structure of his Figure 9 to overcome problems associated with the non-planarity of the structure of his Figure 7. *See* Ismail, p. 511, left column. Thus, even if selective etching were

used to define the structure of Figure 7, as suggested by the Examiner, Ismail would not suggest forming a gate dielectric in a structure formed by use of selective etching, as required by independent claim 46. In fact, Ismail teaches that the use of gate dielectrics is incompatible with his non-planar structure of his Figure 7, reserving such use only for the planar structure of his Figure 9. Thus, any inference by the Examiner that the use of gate dielectrics is compatible with the structure in Ismail's Figure 7 is not based on the reference itself, but rather is impermissible hindsight based on Applicants' disclosure. Similarly, the formation of MOSFETs (i.e., devices incorporating a gate dielectric) on a structure with SiGe selectively removed, as required by dependent claims 41 and 43, is neither taught nor suggested by the cited art.

Further, Applicants submit that none of the cited art teaches or suggests selective removal of SiGe by thermal oxidation, as required by dependent claim 36. Rather, Chang discloses removal of SiGe only by chemical etching. *See* Chang, Abstract. Moreover, none of the cited art teaches or suggests a MOSFET comprising a high-k dielectric (i.e., one with a dielectric constant higher than that of SiO_2), as required by dependent claims 42, 44, and 55. Rather, as recognized by the Examiner, Ismail discloses only an SiO_2 insulator layer, and only in a planar structure incompatible with selective removal techniques (as described above). *See* Ismail, p. 511, left column and Figure 9. None of the cited art teaches or suggests a method of forming a surface channel device and a buried channel device wherein a single strained layer comprises the channel of each, as required by dependent claim 45. Rather, Ismail teaches that his complementary MODFET structure requires that electrons flow through a strained Si layer and holes flow through a strained SiGe layer. *See* Ismail, page 510, right column, last paragraph, and Figure 7.

Applicants submit that, for at least these reasons, independent claims 33 and 46, and claims dependent therefrom, are patentable over the cited prior art.

CONCLUSION

In light of the foregoing, Applicants respectfully submit that all claims are now in condition for allowance.

If the Examiner believes that a telephone conversation with Applicants' attorney would expedite allowance of this application, the Examiner is cordially invited to call the undersigned attorney at (617) 570-1806.

No fees are believed necessary for the filing of this Response. However, if any fees are due, the Director is hereby authorized to charge such fees to our Deposit Account No. 07-1700, under Order No. ASC-057C1.

Respectfully submitted,

Date: April 9, 2008
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